



- Drafts
- Pending
- Active
 - L1: (259) memory and substrate and trench and memory near cells1 and trench near line
 - L2: (187) memory and substrate and trench and memory near cells1 and trench near line and gate an...
 - L3: (59) memory near flash and substrate and trench and memory near cells1 and trench near line a...
 - L4: (4) memory near flash and substrate and trench and memory near cells1 and trench adj line and...
 - L5: (16) memory and substrate and trench and memory near cells1 and trench adj line and gate and...
 - L6: (6) memory near flash and substrate and trench adj line
 - L7: (13) (first adj2 column) with trench
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Default operator: OR Highlight all hit terms initially

(first adj2 column) with trench

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| | U | I | Document ID | Issue Date | Pages | Title | Current OR | Current XRef |
|----|-------------------------------------|--------------------------|-------------------|------------|-------|---|------------|--|
| 1 | <input type="checkbox"/> | <input type="checkbox"/> | US 20050123257 A1 | 20050609 | 11 | Optical fiber of complex index profile | 385/127 | |
| 2 | <input checked="" type="checkbox"/> | <input type="checkbox"/> | US 20050017283 A1 | 20050127 | | Semiconductor device | 257/301 | |
| 3 | <input checked="" type="checkbox"/> | <input type="checkbox"/> | US 20030180020 A1 | 20030925 | | Optical fiber of complex index profile | 385/127 | |
| 4 | <input checked="" type="checkbox"/> | <input type="checkbox"/> | US 20030169629 A1 | 20030911 | | Semiconductor memory cell configuration and a method for producing the configuration | 365/200 | 257/E21.652 |
| 5 | <input checked="" type="checkbox"/> | <input type="checkbox"/> | US 20030096429 A1 | 20030522 | | Laser-induced cell lysis system | 436/174 | 422/99; 436/63 |
| 6 | <input checked="" type="checkbox"/> | <input type="checkbox"/> | US 6904216 B2 | 20050607 | | Optical fiber of complex index profile | 385/127 | |
| 2 | <input checked="" type="checkbox"/> | <input type="checkbox"/> | US 6853023 B2 | 20050208 | | Semiconductor memory cell configuration and a method for producing the configuration | 257/301 | 257/302; 257/774; 257/E21.652 |
| 8 | <input checked="" type="checkbox"/> | <input type="checkbox"/> | US 6815209 B2 | 20041109 | | Laser-induced cell lysis system | 436/63 | 422/99; 435/287.1; 435/290 |
| 9 | <input checked="" type="checkbox"/> | <input type="checkbox"/> | US 6566691 B1 | 20030520 | | Semiconductor device with trench gate having structure to promote conductivity modulation | 257/139 | 257/133; 257/330; 257/E21.384 |
| 10 | <input checked="" type="checkbox"/> | <input type="checkbox"/> | US 5529944 A | 19960625 | | Method of making cross point four square folded bitline trench DRAM cell | 438/242 | 257/E21.652; 257/E27.096; 438/246 |
| 11 | <input checked="" type="checkbox"/> | <input type="checkbox"/> | US 5173436 A | 19921222 | | Method of manufacturing an EEPROM with trench-isolated bitlines | 438/262 | 257/E21.209; 257/E21.552; 257/E21.68 |

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